Control Logic																					
Instruction	State #	Condition	Data Path	PCen	PCLD	Aen	Aout	IRen	Ten	Tout	ALUout	ALUM	ROMout	DEV1en	DEV2en	DEV0en	MEMen	MEMin	MEMout	ALUCn	Examples	Encoding
FETCH	**S0**	**X**	**ROM -> IR**					0				X	0							X	/	/
	S1	**X**	**PC+1 -> PC**	0								X								X	/	/
OUT	**S2**	**OPC=0 & OPC2=0**	**A -> DEV1**				0					X		0						X	*OUT DEV1, A*	*20*
		OPC=0 & OPC2=1	**A -> DEV2**												0						*OUT DEV2, A*	*24*
		OPC=1 & OPC2=0	**T -> DEV1**							0				0							*OUT DEV1, T*	*28*
		OPC=1 & OPC2=1	**T -> DEV2**												0						*OUT DEV2, T*	*2C*
IN	**S3**	**OPC=0**	**DEV0 -> A**			0						X				0				X	*IN A*	*30*
		OPC=1	**DEV0 -> T**						0												*IN T*	*38*
LDR	**S4**	**/**	**RAM -> A**			0						X					0		0	X	*LDR 0x123*	*41 23*
	S5	**/**	**PC+1 -> PC**	0								X								X		
SUB*	**S6**	**OPC=0**	**A-T -> A**			0					0	0								0	*SUB A*	*60*
		OPC=1	**A-T -> T**						0												*SUB T*	*68*
LDI	**S7**	**OPC=0**	**ROM -> A**			0						X	0							X	*LDI A, #0xAB*	*70 AB*
		OPC=1	**ROM -> T**						0												*LDI T, #0xEF*	*78 EF*
	S8	**/**	**PC+1 -> PC**	0								X								X	/	/
ADD*	**S9**	**OPC=0**	**A+T -> A**			0					0	0								1	*ADD A*	*90*
		OPC=1	**A+T -> T**						0												*ADD T*	*98*
JMP	**S10 (A)**	**/**	**IR+ROM -> PC**		0							X	0							X	*JMP 0x123*	*A1 23*
AND*	**S11 (B)**	**OPC=0**	**A&T -> A**			0					0	1								X	*AND A*	*B0*
		OPC=1	**A&T -> T**						0												*AND T*	*B8*
STR	**S12 (C)**	**/**	**A -> RAM**				0					X					0	0		X	*STR 0x123*	*C1 23*
	S13 (D)	**/**	**PC+1 -> PC**	0								X								X		
OR*	**S14 (E)**	**OPC=0**	**A | T -> A**			0					0	1								X	*OR A*	*E0*
		OPC=1	**A | T -> T**						0												*OR T*	*E8*
JNZ	**S15 (F)**	**Zflag=0 (A=0)**	**IR+ROM -> PC**	0								X								X	*JNZ 0x123*	*F1 23*
		Zflag=1 (A≠0)	**PC+1 -> PC**		0								0									

Note: (1) All blanks in the table are set to 1, symbol 'X' means don't care, can be 0 or 1.
(2) For all instructions with '*' (i.e., SUB, ADD, AND, and OR), the opcodes are corresponding to 74X181 chip's function code.
(3) All instructions using lower 4 bits of IR register for higher 4 address bits, they cannot make these bits to be any conditions, because these bits are occupied by address.